

Improved Valley-Fill Passive Current Shaper

K. Kit Sum

Consultant

P. O. Box 361110, Milpitas, California 95036-1110

Telephone: (408) 263 7171 +++ Facsimile: (408) 263 7647

Abstract

The original valley-fill current shaper permits input current conduction from 30° to 150° , and then from 210° to 330° . Due to the discontinuities from 0° to 30° and from 150° to 210° , substantial amount of harmonics were introduced into the input current waveform. This article presents an improved version of the valley-fill circuit which extends the conduction angle to near 360° , thus lowering unwanted harmonics as well as improving power line current waveform. Improvements are made with passive components. SPICE simulations compare original circuit with different improved versions of the circuit. 98% power factor is achievable with this new circuit.

Introduction

The valley-fill passive power factor correction circuit was communicated to the author by Spangler [1] in 1988. The idea evolved naturally from work previously performed by Spangler [2]. Subsequent work on this idea was reported in 1991 [3] in which a number of circuits were compared. All the passive circuits came very close to meeting the IEC specification limits. This observation led the author to further investigate the feasibility of providing a minor improvement to the valley-fill circuit to push it into the IEC limits.

Principle of Operation

The original valley-fill circuit is shown in Figure 1. The capacitors C_1 and C_2 are charged in series, and discharged, via the diodes D_5 and D_7 , in parallel. Current is drawn from the line from 30° to 150° , and then from 210° to 330° [†]. Discontinuities occur from 150° to 210° and from 330° to 360° , and then the cycle repeats itself. Diode D_6 is inserted to prevent C_2 from discharging via C_1 . The resistor R_L is a very low value resistor inserted to monitor the input current waveform.

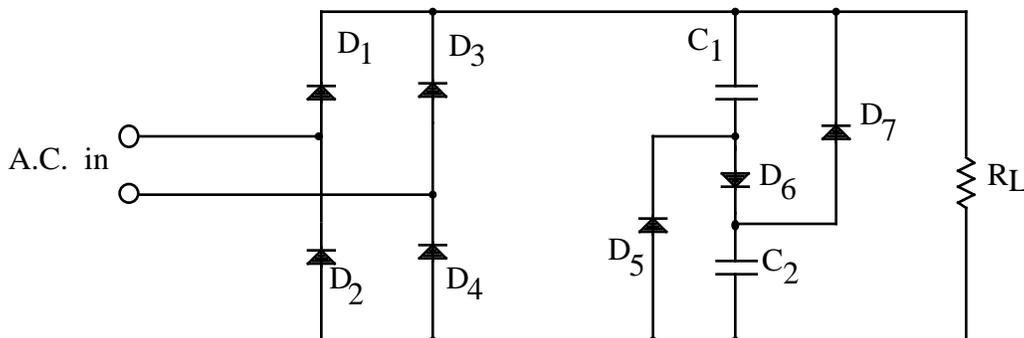


Fig. 1. The Original Valley-Fill Circuit

[†] Assume under steady state condition, the waveform starts from 0° , the sinusoid reaches half of the peak amplitude at 30° , the rest of the half peak locations follows accordingly.

The load R_L is chosen in such a way as to demand a light load for the associated component values, so that a higher harmonic input current wave can be obtained for better comparison. This is based on the idea that a lighter load will have less demand on output current, and as a result, the charges on C_1 and C_2 are not greatly depleted quickly and the resulting charging spike will be narrower than the heavier load counterpart. This effect can easily be verified by experimentally testing or simulation with a heavier load.

Preliminary Observations

Figure 2 shows the input current waveform, from simulation, for the standard or original valley-fill circuit. Discontinuities are observed from 30° to 150° , from 150° to 210° and from 330° to 360° , and then the cycle repeats itself. Much of the input current distortion is caused by these discontinuities which crosses from positive to negative, and then from negative to positive, during each cycle. If this cross-over distortion can be lessened or eliminated, then the likelihood of using this circuit to meet the IEC specifications would be very high. The peak charging spike is also a major contributor of current harmonics, however, since the power content of this spike is not very high, one can conclude that it can be suppressed without too much sacrifice in efficiency.

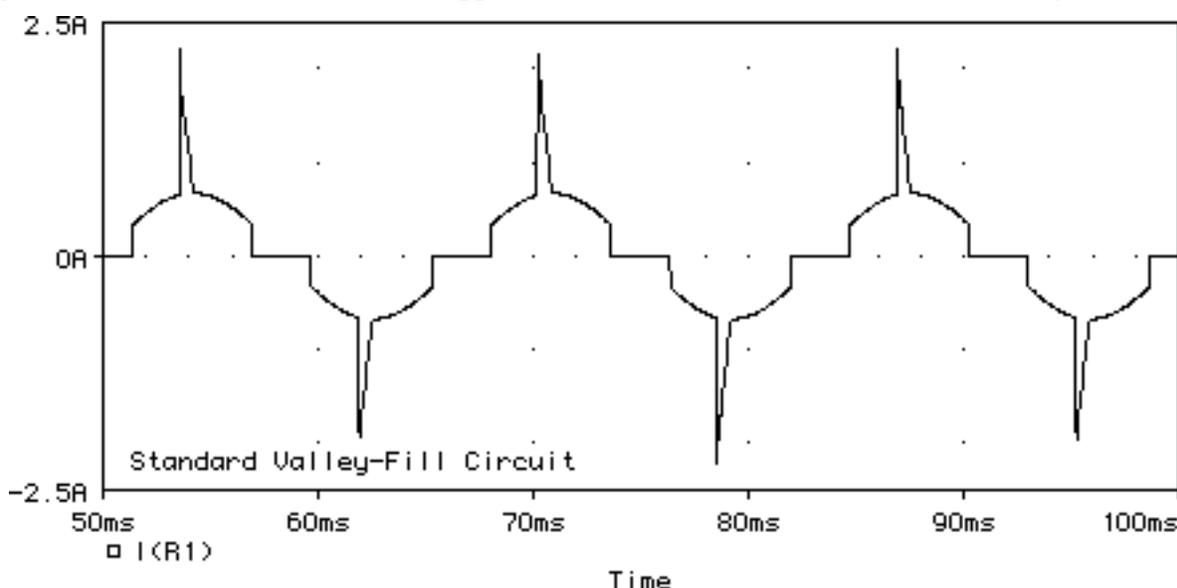


Fig. 2. Standard Valley-Fill Input Current Waveform

For comparison purposes, Table 1 shows the simulated harmonic content of the standard circuit. The total harmonic distortion is seen to be close to 35%. Figure 3 shows the Fourier plot of the harmonics.

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	6.000E+01	7.425E-01	1.000E+00	1.547E+00	0.000E+00
2	1.200E+02	2.069E-03	2.786E-03	-1.726E+01	-1.880E+01
3	1.800E+02	1.905E-01	2.566E-01	-1.655E+02	-1.671E+02
4	2.400E+02	1.189E-03	1.601E-03	2.445E+01	2.290E+01
5	3.000E+02	7.131E-02	9.604E-02	1.037E+02	1.021E+02
6	3.600E+02	8.807E-04	1.186E-03	-8.717E+00	-1.026E+01
7	4.200E+02	1.303E-01	1.755E-01	-1.354E+02	-1.370E+02
8	4.800E+02	2.368E-03	3.189E-03	-1.709E+02	-1.725E+02
9	5.400E+02	9.409E-02	1.267E-01	7.783E+01	7.628E+01
TOTAL HARMONIC DISTORTION = 3.492362E+01 PERCENT					

Table 1. Input Current Harmonic Content of Standard Valley-Fill Circuit.

Objectives and Circuit Improvement

To improve the standard circuit, two objectives must be accomplished: 1. Reduce cross-over distortion in the input current waveform; and 2. Suppress charging spike at the peak of the current wave.

To maintain continuous current drawn from the line, the voltage during the cross-over periods must not be less than half of the peak input voltage, at least for most of the cross-over periods. This is because when the capacitors are discharging, they are being discharged in parallel. Only half of the peak line voltage appears across each capacitor.

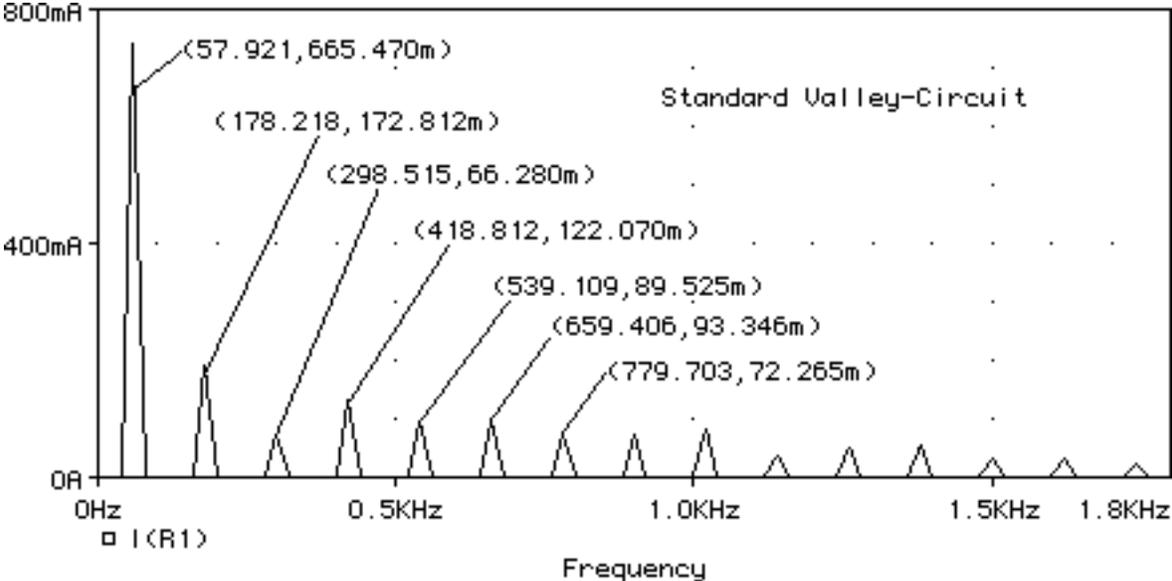


Fig. 3. Standard Valley-Fill Input Current Harmonic Content

(The first number in parenthesis indicate the frequency, the second number is the Fourier component)

Since the bulk of the power is conveyed in the current waveform during conduction time, only a small amount of power will be required to supplement the missing currents during the discontinuities. In other words, the extra power required to fill the gaps is very small compared to the bulk of the power delivered by the valley-fill circuit to the load. Also, during the cross-over periods, the amplitude of the missing part of the waveforms is comparatively small, whereas the main conduction periods have current amplitudes of much higher level.

To maintain the flow of input current, a voltage doubler is inserted to feed the valley-fill circuit. This voltage doubler is configured in such a way as to contribute a very small amount of power to the main circuit, just enough to improve the current waveform at the cross-over points. This means that the capacitors used for the voltage doubler can be orders of magnitude smaller than the values of C_1 and C_2 . Under normal operating conditions, the energy from the voltage doubler is totally absorbed by the main circuit. But during the cross-over periods, the voltage doubler comes into play by continuing to draw current from the line, thus further extending the input current conduction angle.

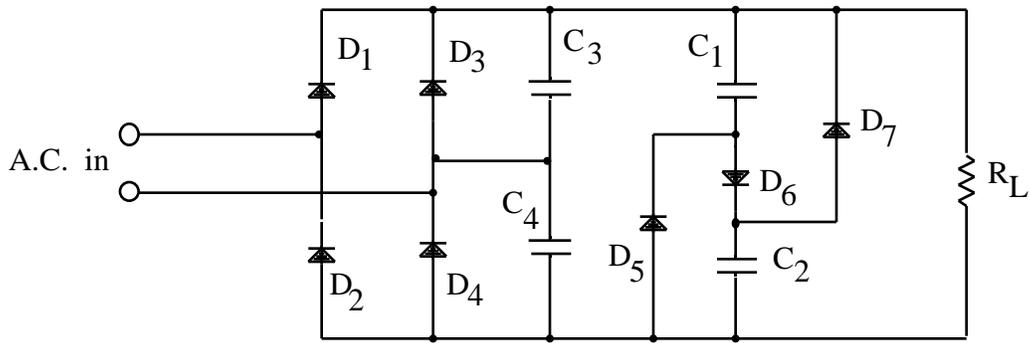


Fig. 4. Valley-Fill Circuit with Voltage Doubler

Figures 5 shows the input current waveform with the improvements at the cross-over points, and Figure 6 is the Fourier plot of the harmonics. However, the peak charging current spike still persists.

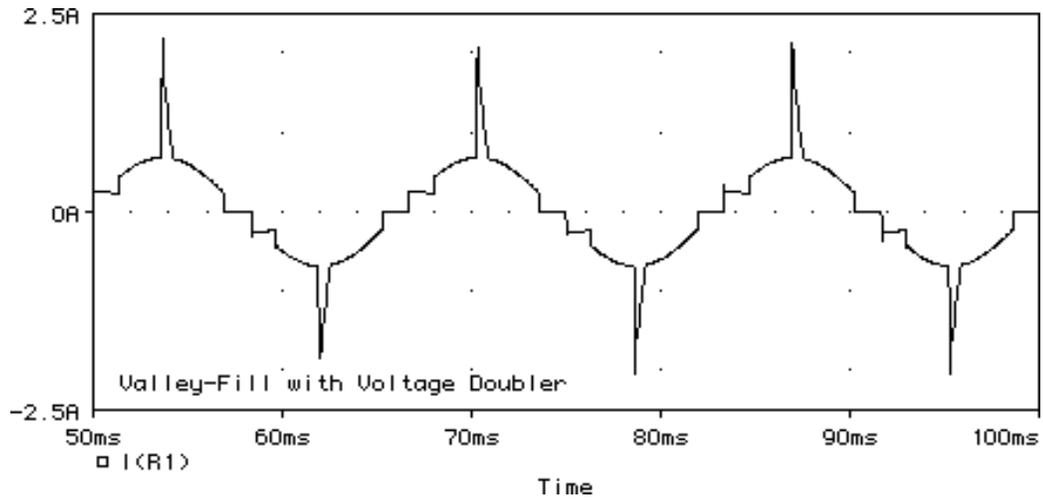


Fig. 5. Valley-Fill with Voltage Doubler

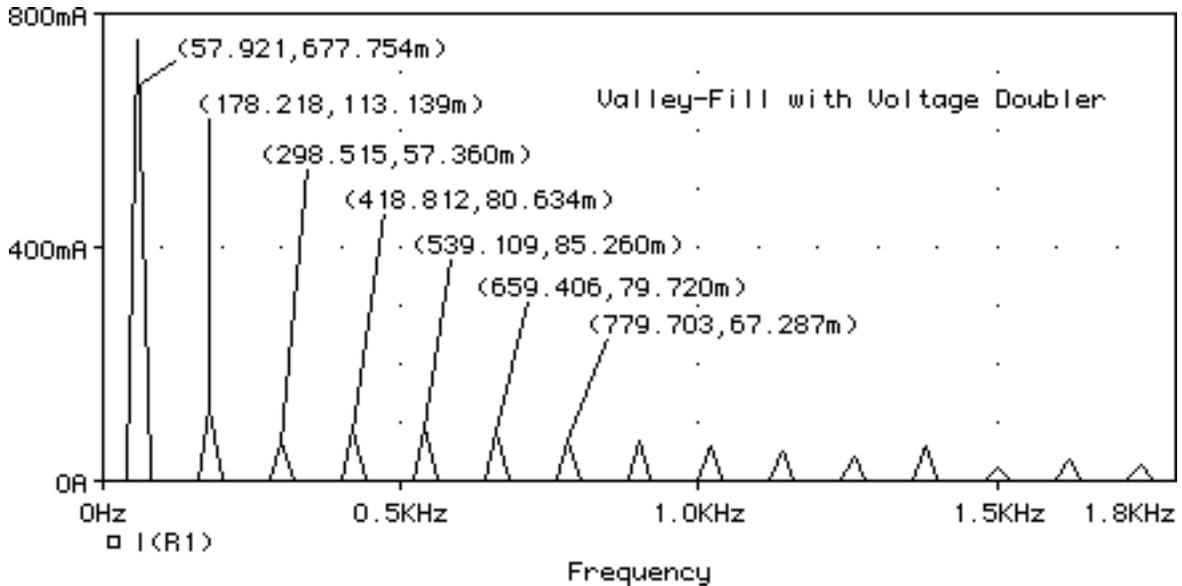


Fig. 6. Harmonic Content of Valley-Fill with Voltage Doubler

(The first number in parenthesis indicate the frequency, the second number is the Fourier component)

To remedy this, a resistor R_{11} is connected to the bottom electrode of C_2 . This is shown in Figure 7. Note that the value of R_{11} is, to some extent, inversely proportional to the output power, since for higher power output, the charging time would be longer, due to a faster rate of charge depletion from capacitors C_1 and C_2 .

Table 2 shows that the total harmonic distortion has been reduced from the standard circuit value of 35% to 9.6% for the voltage doubler with R_{11} .

The current response in Figure 8 can further be improved by the insertion of another resistor R_{12} (shown only on the netlists). Insertion of this resistor (one terminal of the resistor connected to the junction of D_3 and D_4 , and the other terminal connected to the junction of C_3 and C_4) will remove the charging spike at the cross-over points, and further enhance the quality of the input current.

All component values can be found on the netlists provided in this article.

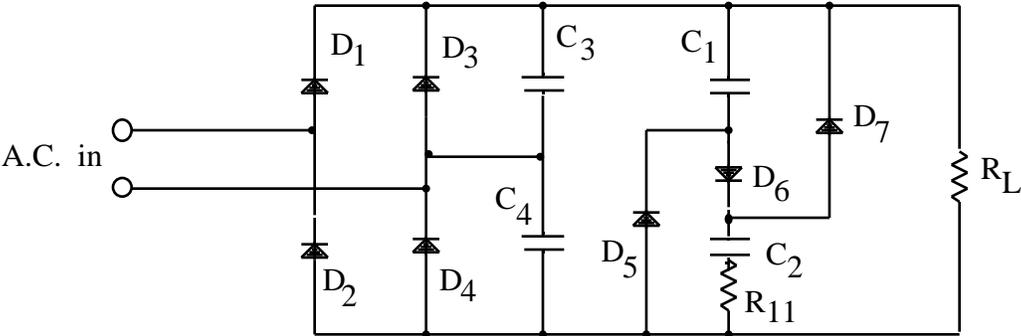


Fig. 7. Valley-Fill Circuit with Voltage Doubler and R_{11} .

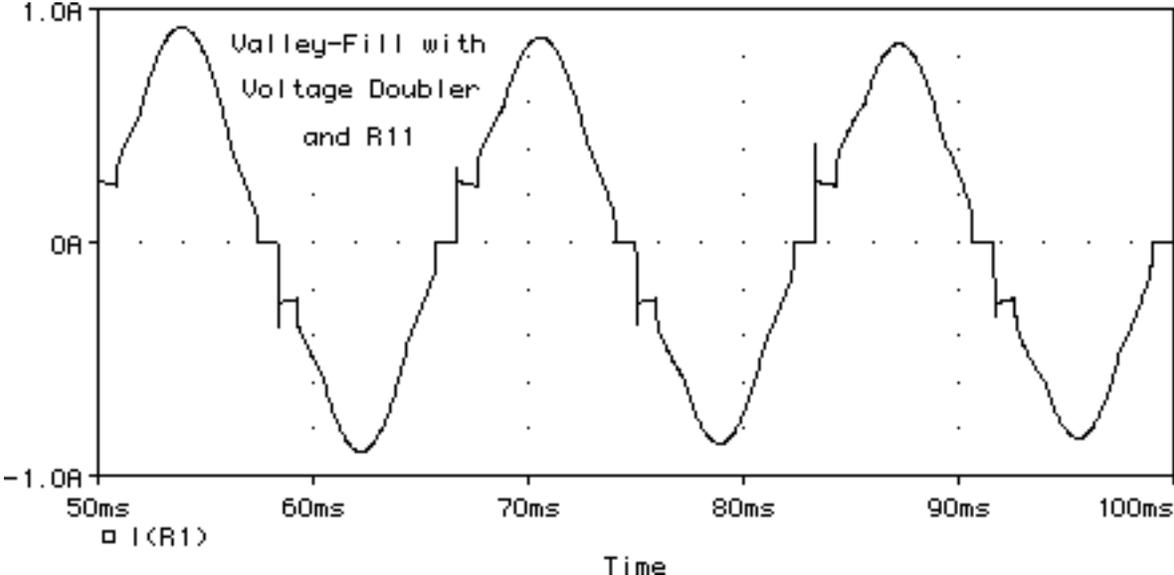


Fig. 8. Input Current Waveform of Valley-Fill Circuit with Voltage Doubler (Fig. 7).

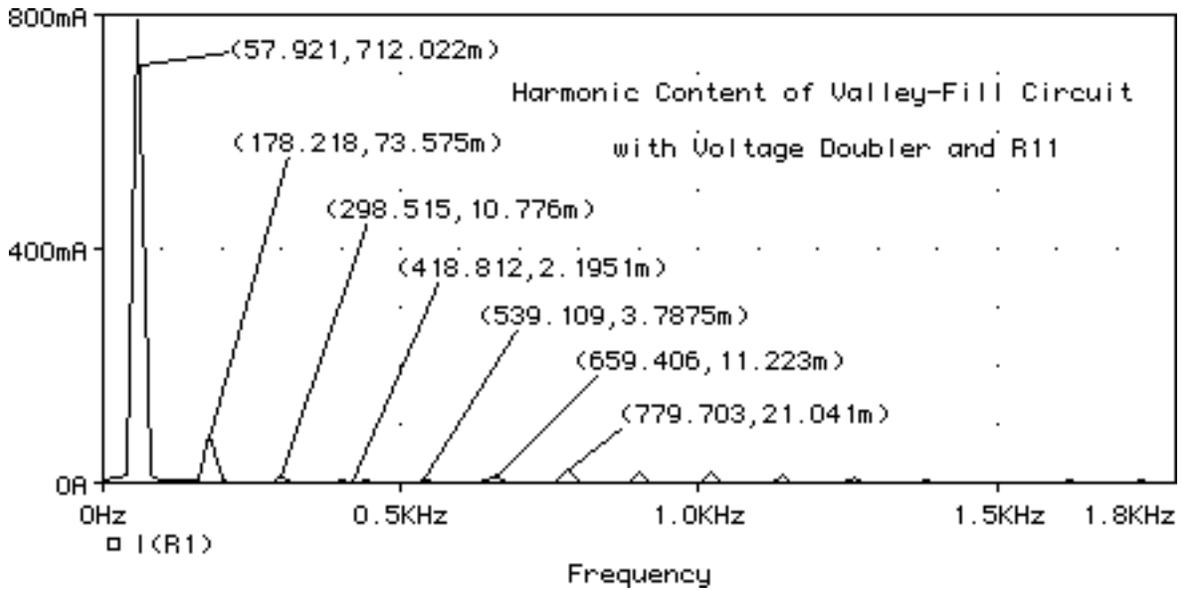


Fig. 9. Input Current Harmonic Content of Valley-Fill with Voltage Doubler and R_{11} .
 (The first number in parenthesis indicate the frequency, the second number is the Fourier component)

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	60	7.666E-01	1.000E+00	9.793E+00	0.000E+00
2	120	3.226E-03	4.208E-03	-8.603E+01	-9.582E+01
3	180	7.234E-02	9.436E-02	-1.764E+02	-1.861E+02
4	240	2.758E-04	3.597E-04	1.577E+02	1.479E+02
5	300	1.193E-02	1.556E-02	9.743E+00	-4.917E-02
6	360	3.751E-04	4.893E-04	-1.012E+02	-1.110E+02
7	420	4.458E-03	5.816E-03	-1.586E+02	-1.684E+02
8	480	2.043E-03	2.665E-03	-8.578E+01	-9.557E+01
9	540	4.200E-03	5.479E-03	-1.342E+02	-1.440E+02

TOTAL HARMONIC DISTORTION (THD) = 9.61 %

Table 2. Input Current Harmonic Content of Valley-Fill Circuit with Voltage Doubler and R_{11} .

IEC Specifications from [3]

The IEC specifications are provided in Table 3 and compared with values in Table 2 in percentages of harmonic shown below:

Harmonic	2nd	3rd	5th	7th	9th	11th	13th	THD*
IEC Limit %	2.00	27.00	10.00	7.00	5.00	3.00	3.00	32.28
Table 2**	0.421	9.436	1.556	0.582	0.548	-	-	9.61

*THD is total harmonic distortion, **Values from Table 2, column 4 **bold** numbers.

Table 3. Comparison of IEC Limits with Simulated Results

Based on this improved current shaper, a circuit for a fluorescent 4-lamp ballast have been built and tested, the measured power factor was found to exceed 98%.

Conclusion and Comments

An improved valley-filled current shaper have been described, simulated, and compared with IEC specification limits. The results indicate a simple and economical solution to a costly problem. This circuit is ideally suited for constant load applications such as fluorescent lamp ballasts. There is a drawback, however, with this current shaper — by design, the input voltage ripple content is very high. Because of this condition, the load is actually deriving power from the *average* of the input voltage.

Employment of this circuit in lamp ballast circuits will result in high output current crest factor, unless square wave switching is used to drive the lamp circuit.

The component values chosen were arbitrary. No attempt was made to optimize the improved circuit for any particular applications. It is, however, reasonable to expect that, after more detailed analysis, a detailed general design approach can be formulated for future use.

The original circuit was originally conceived for economical application in fluorescent lamp ballasts. The market for electronic lamp ballasts demand the circuit to meet various stringent specifications, and yet the component cost must be extremely competitive.

The improved circuit appears simple, yet much more work can be done to set bounds to, say capacitance values for given loads; or to investigate further the efficiency aspect of the circuit performing under variable load conditions.

PSpice® Netlists

```
V-F.cir *** A Passive Power Factor Correction Circuit ***
*** This is the original valley-fill circuit. ***
*** The idea is to widen the current conduction angle, from 30° to
*** 150° range. Simulation performed by K. Kit Sum, October 7, 1996 ***
Vg 1 3 sin(0 170 60 0 0)
R1 1 2 .0001
D1 2 4 Power_Diode
Ra 2 4 1Meg
D2 0 2 Power_Diode
R2 0 2 1Meg
D3 3 4 Power_Diode
R3 3 4 1Meg
D4 0 3 Power_Diode
R4 0 3 1Meg
D5 0 5 Power_Diode
R5 0 5 1Meg
D6 5 6 Power_Diode
*R65 6 1Meg
D7 6 13 Power_Diode
*D94 13 Power_Diode
R13 4 13 .0001
R7 6 13 1Meg
C1 13 5 180uF
C2 6 12 180uF
R1112 0 .0001
**C3 4 14 2.2uF
**C4 14 0 2.2uF
**R12 3 14 330
Ro 4 0 250
.Model D1NX1 D(IS=0.5ua RS=15 BV=70 IBV=.05ua)
.Model Power_DiodeD(RS=.01, CJO=100pF)
.SUBCKT DIODE_WITH_SNUB 101 102
DX 101 102 POWER_DIODE
RSNUB 102 103 1000.0
CSNUB 103 101 0.1uF
```

```
.MODEL POWER_DIODED(RS=0.01, CJO=100pF)
.ENDS
.Tran 50us 100ms 50ms 50us UIC
.Four 60 I(R1)
.Probe
.End
```

© PSpice is a registered trade mark of MicroSim Corporation.

```
V-F.cir *** A Passive Power Factor Correction Circuit ***
*** This circuit functions as a passive power factor corrector. ***
*** The idea is to widen the current conduction angle, from 30° to
*** 150° range. Simulation performed by K. Kit Sum, October 7, 1996 ***
*** This circuit netlist has an additional voltage doubler and a resistor ***
*** R11 connected from the bottom terminal of C2 to ground. ***
```

```
Vg 1 3 sin(0 170 60 0 0)
R1 1 2 .0001
D1 2 4 Power_Diode
Ra 2 4 1Meg
D2 0 2 Power_Diode
R2 0 2 1Meg
D3 3 4 Power_Diode
R3 3 4 1Meg
D4 0 3 Power_Diode
R4 0 3 1Meg
D5 0 5 Power_Diode
R5 0 5 1Meg
D6 5 6 Power_Diode
*R65 6 1Meg
D7 6 13 Power_Diode
*D94 13 Power_Diode
R13 4 13 .0001
R7 6 13 1Meg
C1 13 5 180uF
C2 6 12 180uF
R1112 0 220
C3 4 14 2uF
C4 14 0 2uF
R123 14 .001
Ro 4 0 250
.Model D1NX1 D(IS=0.5ua RS=15 BV=70 IBV=.05ua)
.Model Power_DiodeD(RS=.01, CJO=100pF)
.SUBCKT DIODE_WITH_SNUB 101 102
DX 101 102 POWER_DIODED
RSNUB 102 103 1000.0
CSNUB 103 101 0.1uF
.MODEL POWER_DIODED(RS=0.01, CJO=100pF)
.ENDS
.Tran 50us 100ms 50ms 50us UIC
.Four 60 I(R1)
.Probe
.End
```

References

1. J. J. Spangler, Private telephone communication, 1988.
2. J. J. Spangler, A Power Factor Corrected, MOSFET, Multiple Output, Flyback Switching Supply, *Proc. Tenth Int'l. PCI '85 Conference*, October 22-25, 1985, pp. 19-32.
3. J. Spangler, et al., Electronic Fluorescent Ballast using Power Factor Correction Techniques for Loads Greater than 300 Watts, *Proc. Sixth Annual Applied Power Electronics Conf.*, March 10-15, 1991, Hyatt Regency, Dallas, Texas, pp. 393-399.